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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/691,682

10/22/2003

Shiro Tsunai

17117

6607

23389

7590

12/22/2005

SCULLY SCOTT MURPHY & PRESSER, PC

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EXAMINER

MOTTOLA, STEVEN J

ART UNIT

PAPER NUMBER

2817

DATE MAILED: 12/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.



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42

10/691,682

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
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EXAMINER
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ART UNIT	PAPER
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121905

DATE MAILED:

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Commissioner for Patents

Note attached PTO-1449 and reasons for allowance.

  
Steven J. Mottola  
Primary Examiner

The following is an examiner's statement of reasons for allowance: regarding the rejection of claim 3 in the Chinese office action filed with the IDS of November 4, 2005, while the secondary reference (Japanese patent document 8-274599) is stated to disclose that the second inverter stage 5 is DC coupled to the first inverter stage 4 (fig. 1), it is not clear that this teaching could be applied to the primary reference to Tsunai (fig. 3A) because of the presence of clamp circuit 10 connected to the FET of second inverter stage 15. If the coupling capacitor between the first inverter stage 14 and second inverter stage 15 were removed to meet the "DC-coupled" limitation of line 4 of claim 3, the output of the first stage would be clamped as well as the input of the second stage which would result in substantially altered operation of the circuit.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."